AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1-8. (Canceled)

1
9. (New) Circuitry for use in a differential amplifier, comprising:

an input stage comprising:

a first differential amplifier; and

an offset compensation stage comprising at least one controllable current source, the offset compensation stage being connected to a bias input of the first differential amplifier;

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an output stage comprising a second differential amplifier, the output stage being located after an output of the input stage; and

a programmable resistor network for controlling an amplification of the input stage, the programmable resistor network controlling the amplification in accordance with a feedback from the first differential amplifier.

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10. (New) The circuitry of claim 9, wherein the programmable resistor network comprises resistors connected in series with taps between resistors;

wherein one or more resistors are switchable, via the taps, into a feedback path associated with the first differential amplifier in order to control the amplification.

3 11. (New) The circuitry of claim 9, wherein the first differential amplifier comprises a first operational amplifier and a second operational amplifier;

wherein non-inverting inputs of the first operational amplifier and a second operational amplifier form a symmetric signal input for the first differential amplifier; and

wherein outputs of the first operational amplifier and the second operational amplifier are connected in a feedback path that is connectable to respective inverting inputs of the first operational amplifier and the second operational amplifier.

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4 12. (New) The circuitry of claim 11, wherein the first differential amplifier comprises bias inputs, the bias inputs of the first differential amplifier comprising the inverting input of the first operational amplifier and the inverting input of the second operational amplifier.

5 13. (New) The circuitry of claim 12, wherein the offset compensation stage comprises a bridge circuit, the bridge circuit comprising programmable current sources; and

wherein current taps from connections to the current sources are connected to the bias inputs of the first operational amplifier and the second operational amplifier.

6 14. (New) The circuitry of claim 5, wherein each of the programmable current sources is coupled to a bias input of a corresponding operational amplifier such that each programmable current source can be turned on or off independently.

7 15. (New) The circuitry of claim 1, wherein the second differential amplifier comprises a negative feedback with a programmable resistor which enables an amplification of the output stage to be programmed.

PN 8 16. (New). The circuitry of claim 5, wherein the programmable current sources comprise four programmable current sources.

9 17. (New) The circuitry of claim 8, wherein the four programmable current sources comprise two first current sources connected in series and two second current sources connected in series, the two first current sources and the two second current sources being connected in parallel.

10 18. (New) The circuitry of claim 9, wherein the current taps comprise a first current tap between the two first current sources and a second current tap between the two second current sources.

11 ~~19.~~ 10 (New) The circuitry of claim ~~18~~, wherein the first current tap connects to the bias input of the first operational amplifier, and the second current tap connects to the bias input of the second operational amplifier.

12 ~~20.~~ 2 (New) The circuitry of claim ~~10~~, wherein the first differential amplifier comprises a first operational amplifier and a second operational amplifier;

wherein non-inverting inputs of the first operational amplifier and a second operational amplifier form a symmetric signal input for the first differential amplifier; and

PN wherein outputs of the first operational amplifier and the second operational amplifier are connected in a feedback path that is connectable to respective inverting inputs of the first operational amplifier and the second operational amplifier.

13 ~~21.~~ 12 (New) The circuitry of claim ~~20~~, wherein the first differential amplifier comprises bias inputs, the bias inputs of the first differential amplifier comprising the inverting input of the first operational amplifier and the inverting input of the second operational amplifier.

14 ~~22.~~ 13 (New) The circuitry of claim ~~21~~, wherein the offset compensation stage comprises a bridge circuit, the bridge circuit comprising programmable current sources; and

wherein current taps from connections to the current sources are connected to the bias inputs of the first operational amplifier and the second operational amplifier.

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23. (New) The circuitry of claim ~~22~~, wherein each of the programmable current sources is coupled to a bias input of a corresponding operational amplifier such that each programmable current source can be turned on or off independently.

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24. (New) The circuitry of claim ~~23~~, wherein the second differential amplifier comprises a negative feedback with a programmable resistor which enables an amplification of the output stage to be programmed.